CY7C1019BN

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12, 15 ns**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**
- **Functionally equivalent to CY7C1019**

Functional Description

The CY7C1019BN is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

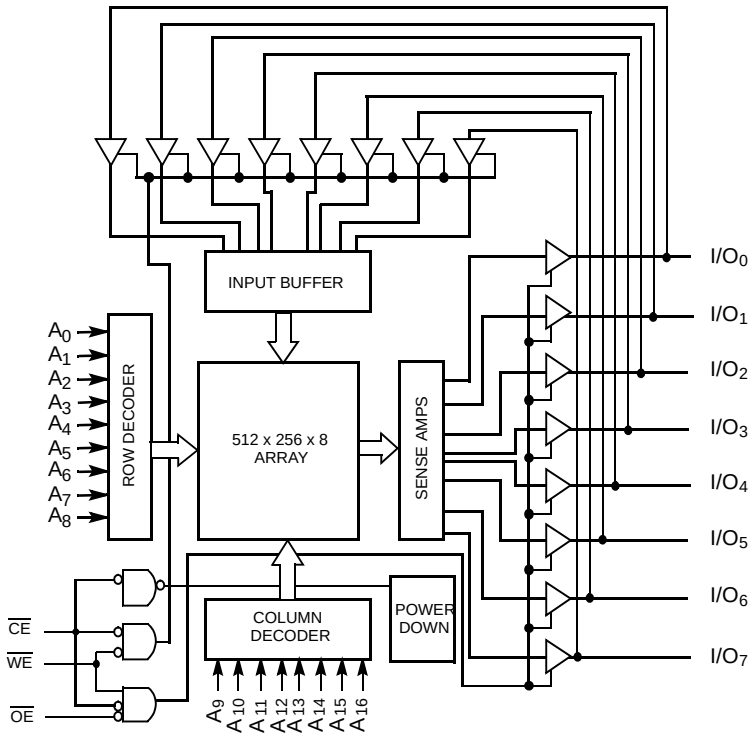
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1019BN is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ packages.

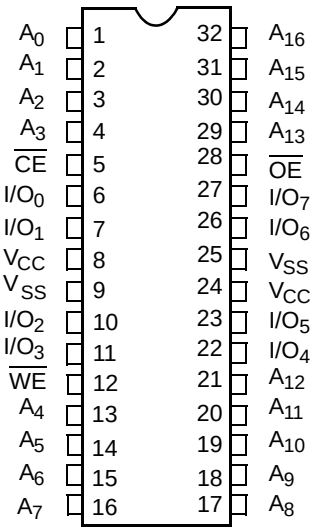
Logic Block Diagram



Pin Configurations

SOJ / TSOPII

Top View



Selection Guide

		7C1019BN-12	7C1019BN-15	Unit
Maximum Access Time		12	15	ns
Maximum Operating Current		140	130	mA
Maximum Standby Current		10	10	mA
	L	1	1	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

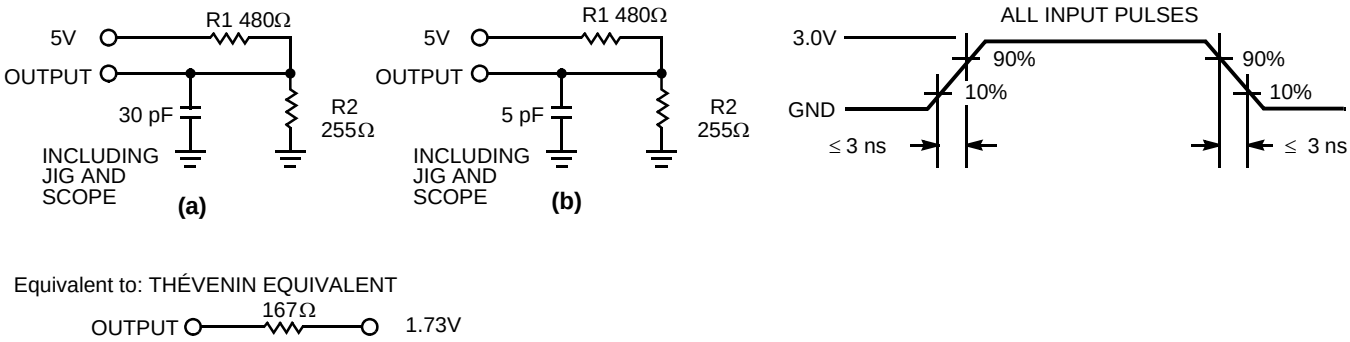
Parameter	Description	Test Conditions		-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}			140		130	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40	mA
			L		20		20	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			10		10	mA
			L		1		1	

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics[4] Over the Operating Range

Parameter	Description	-12		-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15	ns
Write Cycle[7, 8]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		6		7	ns

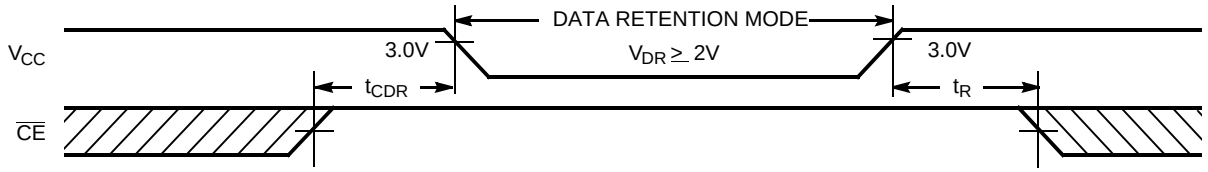
Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

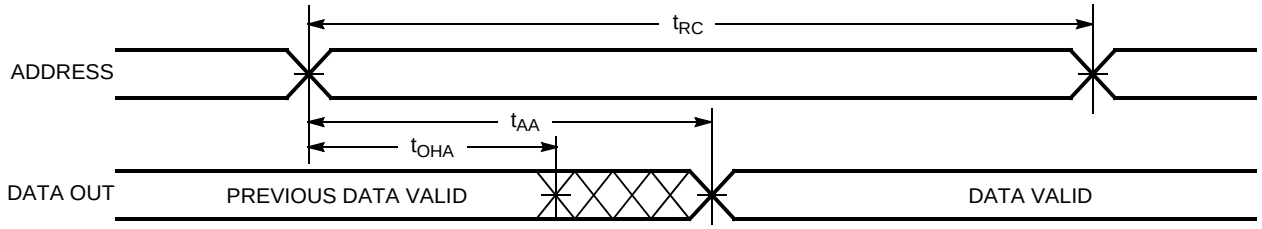
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed V_{CC} + 0.5V $V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current			300	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		200		µs

Data Retention Waveform

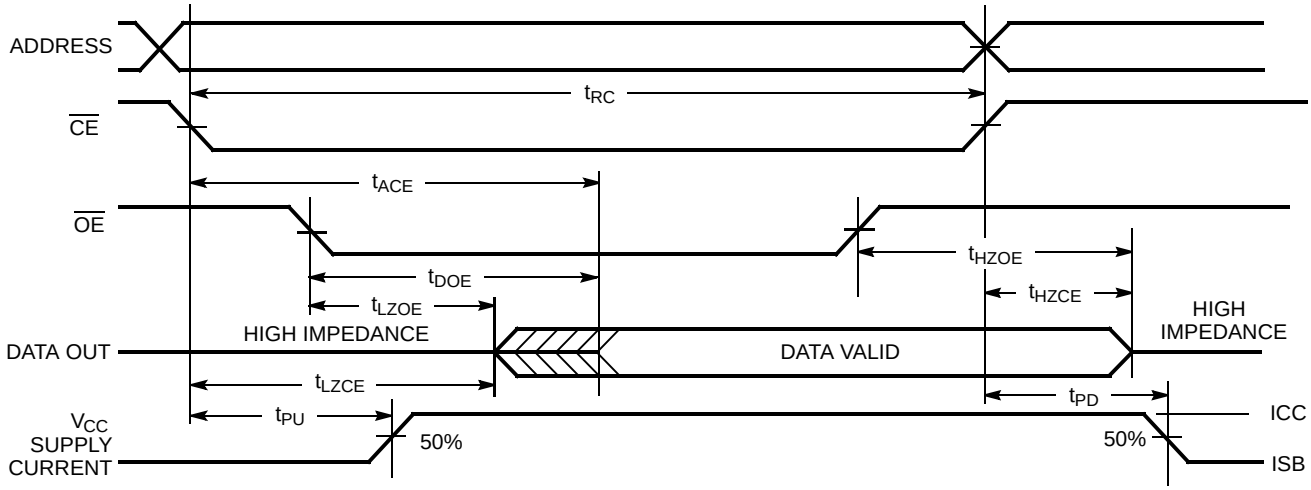


Switching Waveforms

Read Cycle No. 1[9, 10]



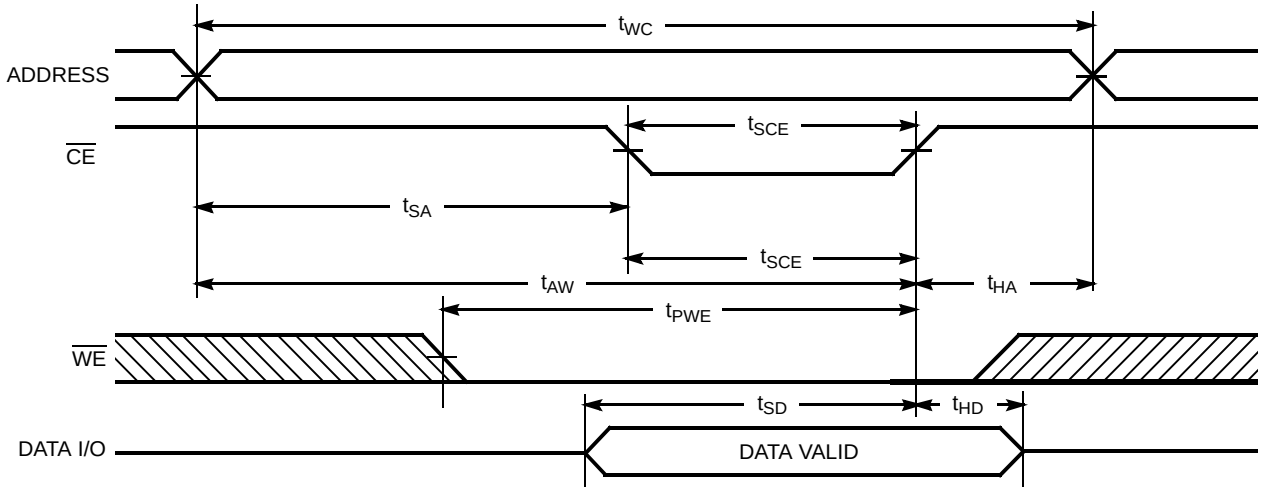
Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



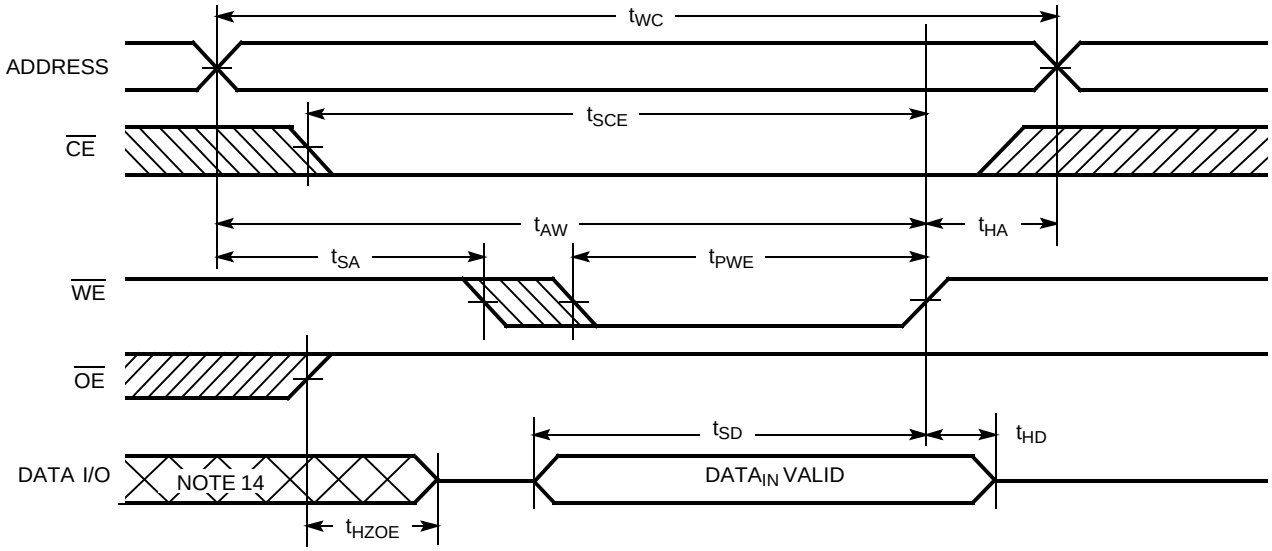
Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. WE is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]



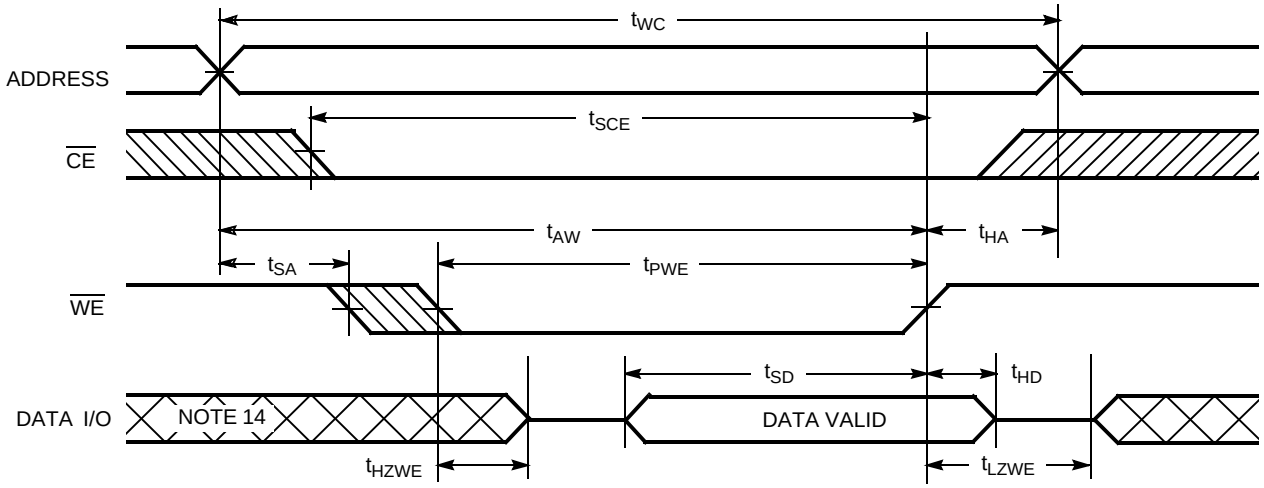
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[12, 13]



Notes:
12. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[13]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

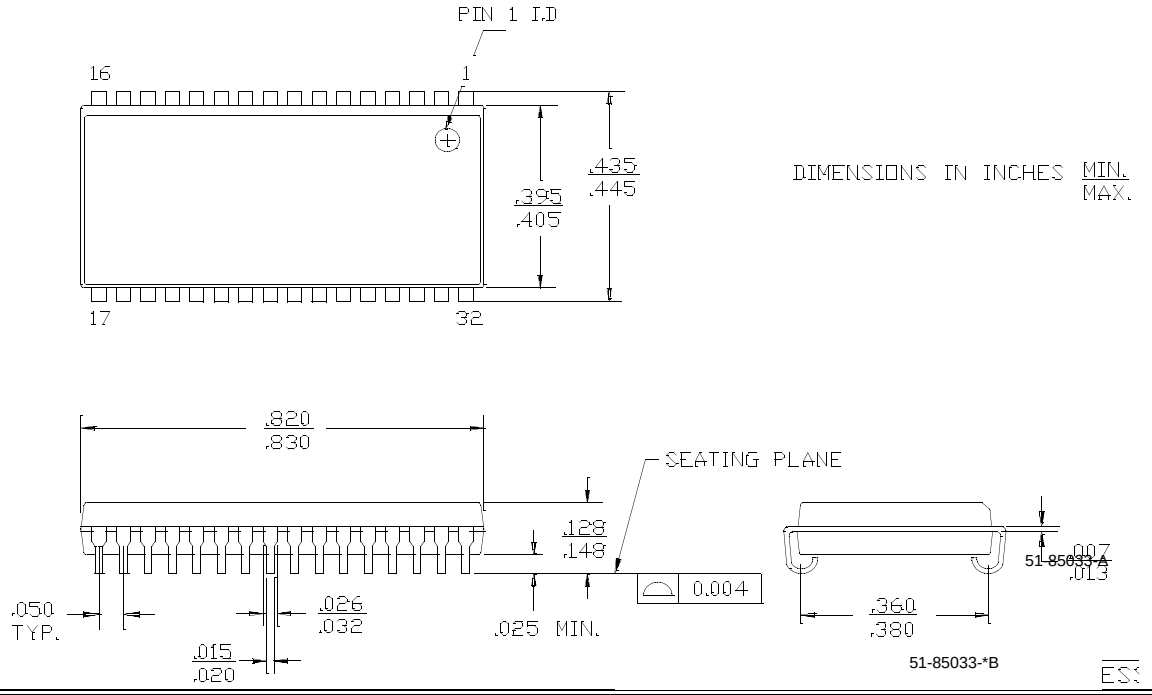
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1019BN-12VC	51-85033	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019BN-12ZC	51-85095	32-Lead TSOP Type II	
	CY7C1019BN-12ZXC	51-85095	32-Lead TSOP Type II (Pb-free)	
15	CY7C1019BN-15VC	51-85033	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019BN-15ZXC	51-85095	32-Lead TSOP Type II (Pb-free)	

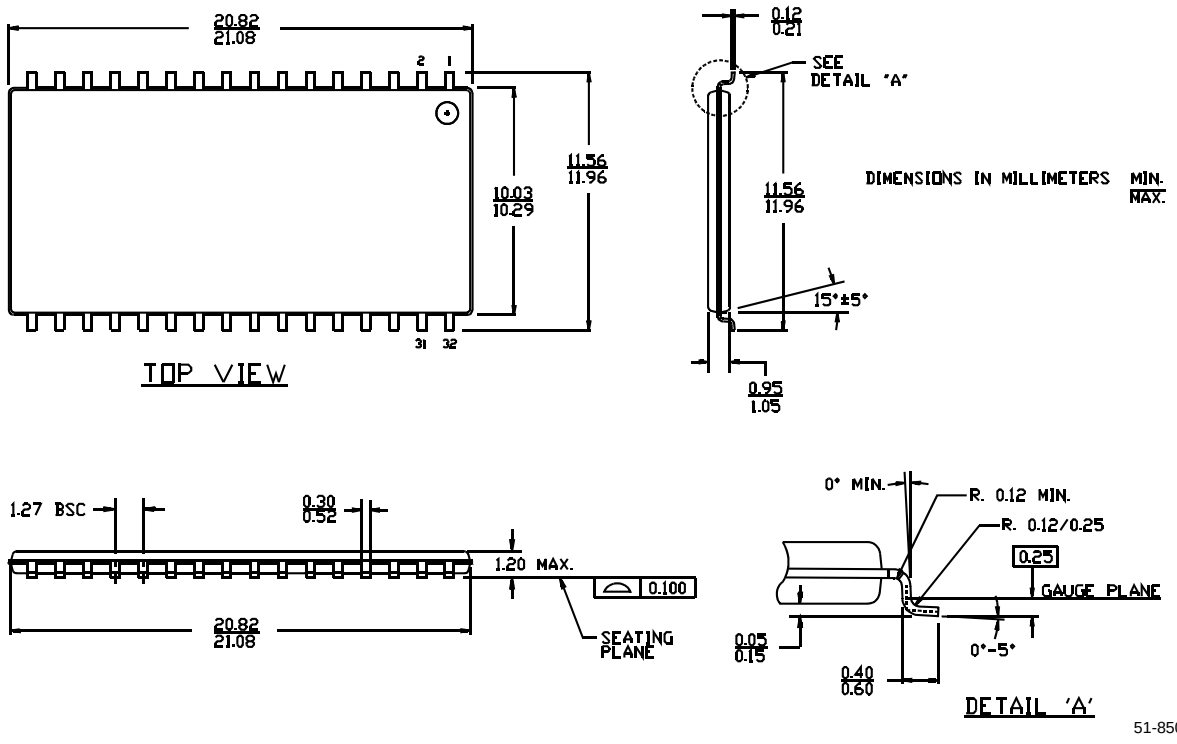
Please contact local sales representative regarding availability of these parts

Package Diagrams

32-pin (400-mil) Molded SOJ (51-85033)



32-pin TSOP II (51-85095)



Document History Page

Document Title: CY7C1019BN 128K x 8 Static RAM Document Number: 001-06425				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	423847	See ECN	NXR	New Data Sheet